AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory apparatus comprising:

a rewritable nonvolatile memory; and

a control circuit,

wherein the rewritable nonvolatile memory includes a plurality of memory cells arranged in a memory array,

wherein the memory apparatus brings logical addresses into correspondence with physical addresses of the rewritable nonvolatile memory, and retains a piece of number-of-rewrites information for each logical address,

wherein a memory cell associated with each logical address includes a piece of memory information,

wherein the control circuit can perform [[a]] replacement ~~process~~ of [[a]] the piece of memory information ~~on~~ in the rewritable nonvolatile memory, ~~and~~

wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the ~~pieces~~ associated piece of number-of-rewrites information with a second physical address, so as to bring

the given logical address into ~~another~~ correspondence with the second physical address, and performing data transfer according to the replacement.

2. (Original) The memory apparatus of Claim 1, wherein the second physical address is a free physical address used for a correspondence with no logical address.

3. (Original) The memory apparatus of Claim 1,

wherein the second physical address is a physical address corresponding to a second logical address of the logical addresses, having a larger number of rewrites in comparison to the given logical address having the small number of rewrites, and

wherein the second logical address is changed so as to be brought into correspondence with the first physical address to which the given logical address having the small number of rewrites was assigned.

4. (Original) The memory apparatus of Claim 1, wherein the replacement process can be performed concurrently with a process in response to a direction for writing provided from an outside of a memory card.

5. (original) The memory apparatus of Claim 4, wherein the replacement process can be performed when the number of rewrites of the logical address targeted for the process in response to the direction for writing reaches a given number of times.

6. (Original) The memory apparatus of Claim 5, wherein the replacement process can be performed on a logical address having a smallest number of rewrites, of arbitrarily extracted logical addresses.

7. (Currently Amended) The memory apparatus of Claim 4, wherein, during the process in response to the direction for writing, the control circuit brings ~~the~~ a logical address targeted for the process into correspondence with a third physical address and performs data rewrite.

8. (Currently Amended) The memory apparatus of Claim [[7]]1, wherein the nonvolatile memory has an address translation table in which correspondences of the logical addresses and physical addresses are defined.

9. (Currently Amended) The memory apparatus of Claim 8, wherein the piece of number-of-rewrites information

for each logical address is retained in a region of the physical address corresponding to the logical address.

10. (Currently Amended) The memory apparatus of Claim 8, wherein the piece of number-of-rewrites information for each logical address is retained in a number-of-rewrites table.

11. (Currently Amended) A memory card comprising:

a rewritable nonvolatile memory; and

a control circuit,

wherein the rewritable nonvolatile memory includes a plurality of memory cell transistors arranged in a memory array arranged,

wherein the memory card brings logical addresses into correspondence with physical addresses of the rewritable nonvolatile memory, and retains a piece of number-of-rewrites information for each logical address,

wherein a memory cell transistor associated with each logical address has a piece of memory information,

wherein the control circuit can ~~executes~~ execute a rewrite process of the rewritable nonvolatile memory in response to a direction for writing from an outside, and a

replacement process of memory information on the rewritable nonvolatile memory, and

wherein the replacement process is a process of replacing a first physical address corresponding to a given logical address judged to have a small number of rewrites based on the ~~pieces~~ associated piece of number-of-rewrites information with a second physical address so as to bring the given logical address into ~~another~~ correspondence with the second physical address, and performing data transfer according to the replacement.

Claims 12-17(Cancelled)

18. (New) The memory apparatus of Claim 1,

wherein the memory array has a plurality of word lines and a plurality of bit lines connected to the memory cells, and

wherein a memory cell targeted for rewrite shares a word line or a bit line with a memory cell not targeted for rewrite.

19. (New) The memory apparatus of Claim 11,

wherein the memory array has a plurality of word lines and a plurality of bit lines connected to the memory cell transistors, and

wherein a memory cell transistor targeted for rewrite shares a word line or a bit line with a memory cell transistor not targeted for rewrite.